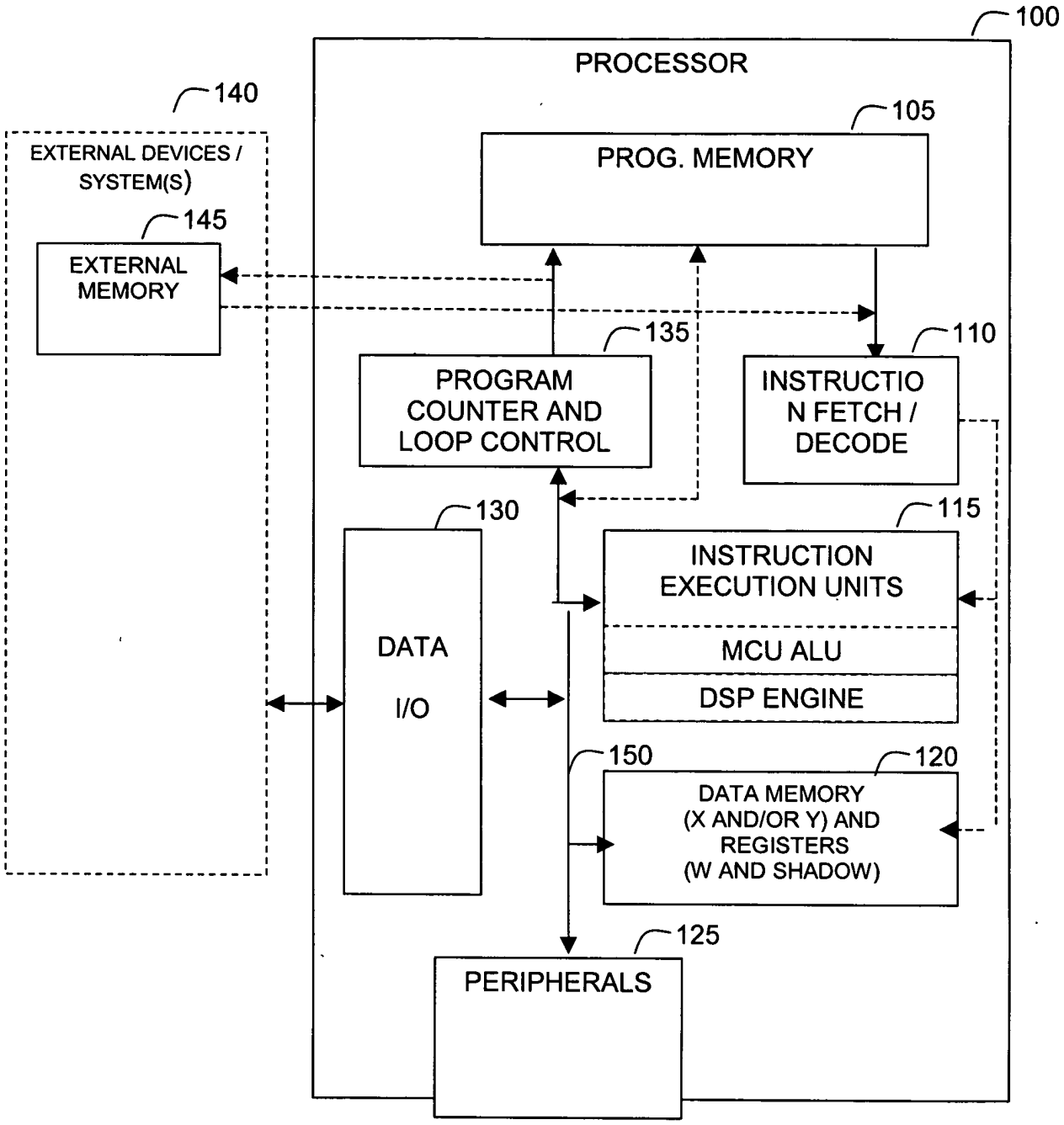
100
PROCESSOR
140
EXTERNAL DEVICES / SYSTEM(S)
145
EXTERNAL MEMORY
105
PROG. MEMORY
135
PROGRAM COUNTER AND LOOP CONTROL
110
INSTRUCTIO N FETCH / DECODE
130
DATA I/O
115
INSTRUCTION EXECUTION UNITS
MCU ALU
DSP ENGINE
150
120
DATA MEMORY (X AND/OR Y) AND REGISTERS (W AND SHADOW)
125
PERIPHERALS

FIG. 1

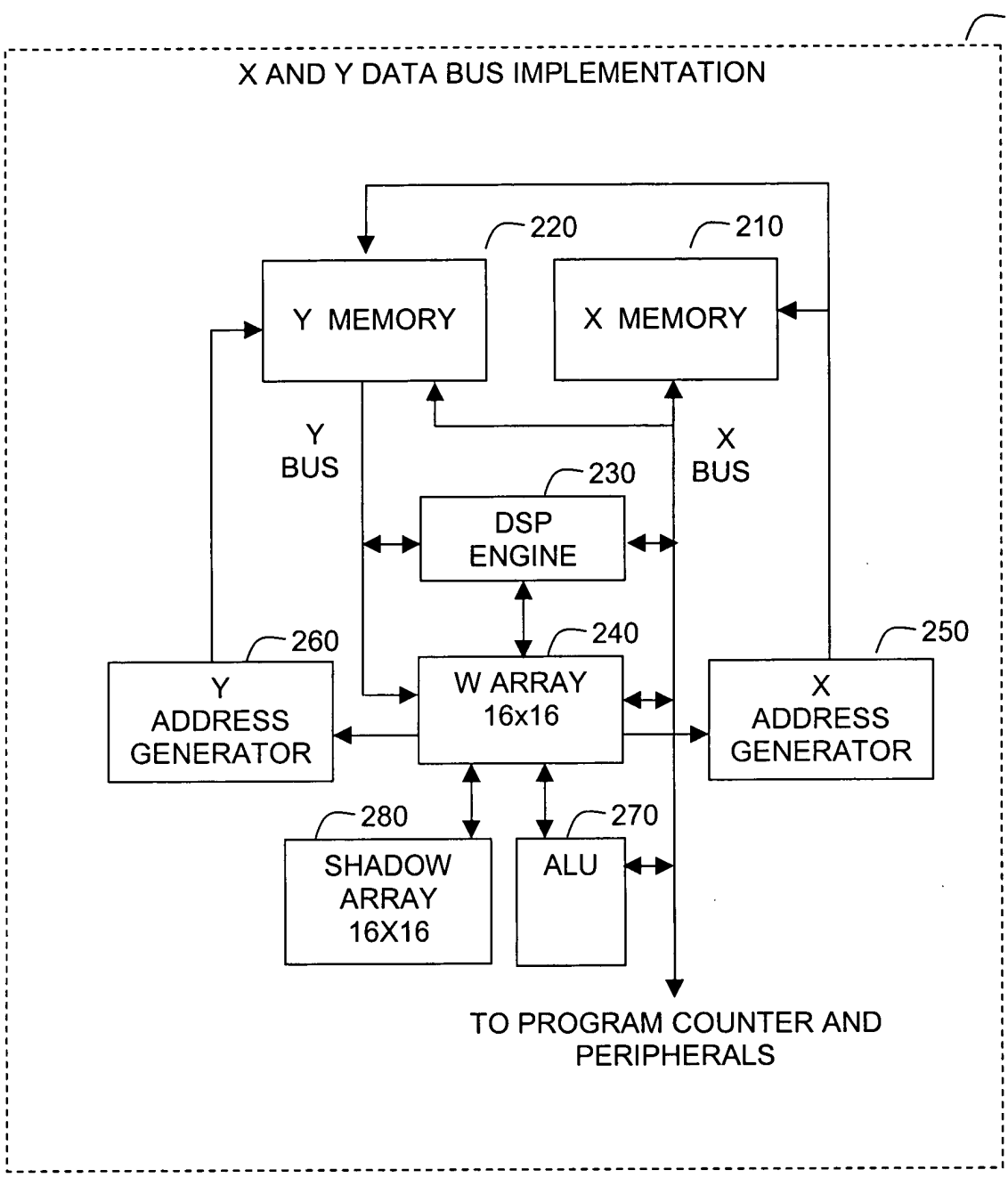
100
X AND Y DATA BUS IMPLEMENTATION
220
210
Y MEMORY
X MEMORY
Y
BUS
X
BUS
230
DSP
ENGINE
260
240
250
Y
ADDRESS
GENERATOR
W ARRAY
16x16
X
ADDRESS
GENERATOR
280
270
SHADOW
ARRAY
16X16
ALU
TO PROGRAM COUNTER AND
PERIPHERALS

FIG. 2

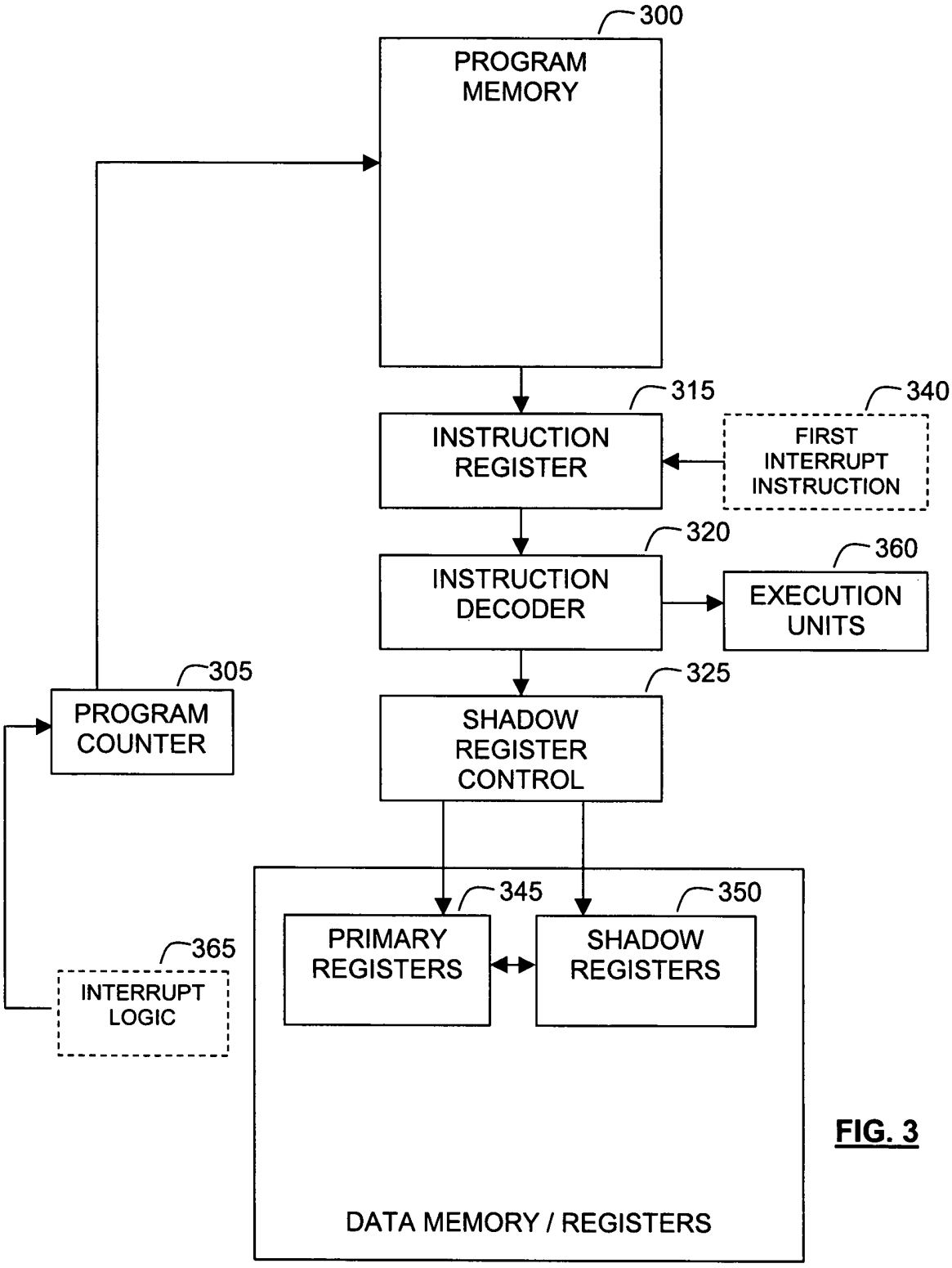
300
PROGRAM MEMORY
315
INSTRUCTION REGISTER
340
FIRST INTERRUPT INSTRUCTION
320
INSTRUCTION DECODER
360
EXECUTION UNITS
305
PROGRAM COUNTER
325
SHADOW REGISTER CONTROL
345
PRIMARY REGISTERS
350
SHADOW REGISTERS
365
INTERRUPT LOGIC
DATA MEMORY / REGISTERS

FIG. 3

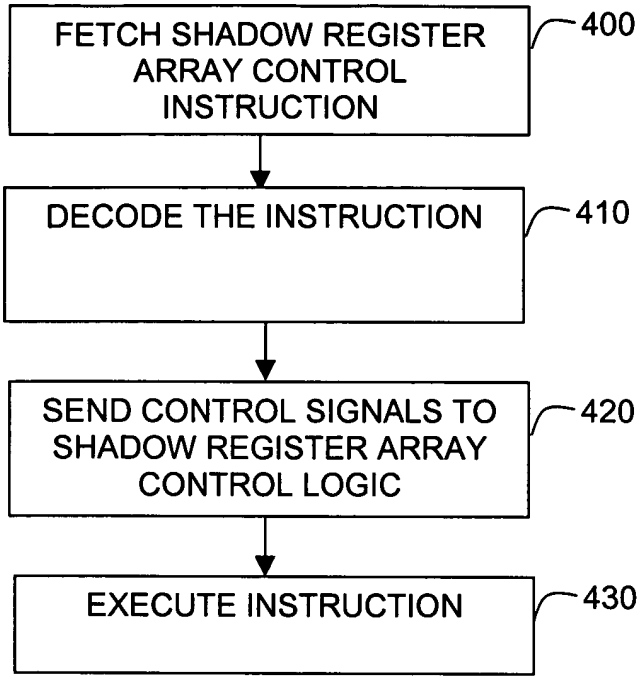
FETCH SHADOW REGISTER ARRAY CONTROL INSTRUCTION
400
DECODE THE INSTRUCTION
410
SEND CONTROL SIGNALS TO SHADOW REGISTER ARRAY CONTROL LOGIC
420
EXECUTE INSTRUCTION
430

FIG. 4A

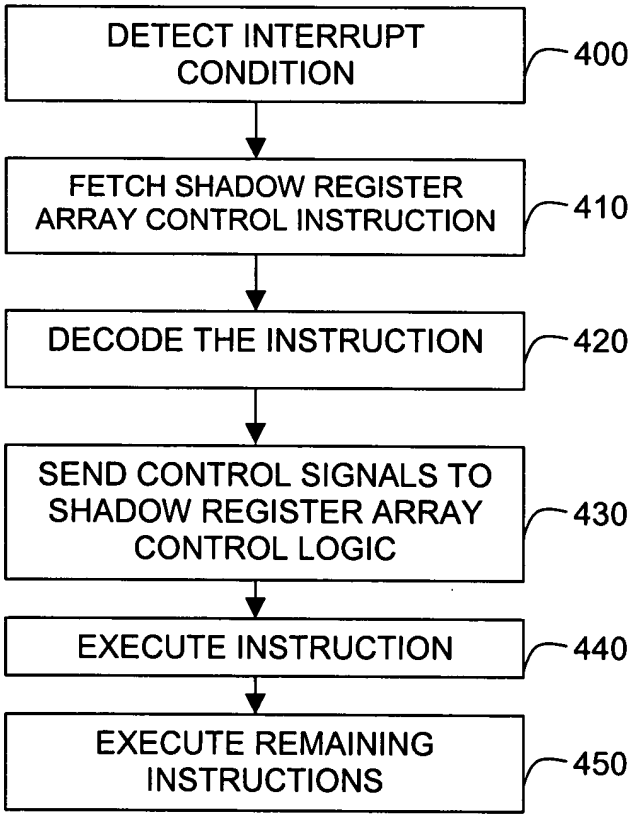
DETECT INTERRUPT CONDITION
400
FETCH SHADOW REGISTER ARRAY CONTROL INSTRUCTION
410
DECODE THE INSTRUCTION
420
SEND CONTROL SIGNALS TO SHADOW REGISTER ARRAY CONTROL LOGIC
430
EXECUTE INSTRUCTION
440
EXECUTE REMAINING INSTRUCTIONS
450

FIG. 4B

SYNTAX	ENCODING						DESCRIPTION
POP.S	1111	1110	1000	0000	0000	0000	write values in shadow to primary
PUSH.S	1111	1110	1010	0000	0000	0000	write values in primary to shadow

5,765,009 "6/26/98

FIG. 5